II Semester [VLSI Design & Embedded Syst

USN | | | | | | | | | | |

12EC047

M.Tech. Degree Examination, Dec.2013/Jan.2014
Low Power VLSI Design

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions.***
2. ***Answer in brief with design, example wherever relevant.***

1 a. Explain the need for low power consumption in VLSI designs. **(08 Marks)**

b. Explain in brief the following effects of influencing Threshold voltage in submicron MOSFET devices:
(i) Short channel length effect.
(ii) Narrow gate wide effects.
(iii) Reverse short channel effect. **(12 Marks)**

2 a. With usual notation, derive the expression for dynamic power dissipation in CMOS inverter. **(10 Marks)**

b. Discuss the impact of technology scaling device innovations to achieve low power and high speed designs. **(10 Marks)**

3 a. Explain the concept of gate level power estimation with an example of 2 input NAND gate. Extend it to gate level power analysis flow. **(10 Marks)**

b. Identify the characteristics of architecture level design representation and name some building blocks of design at architectural level. Discuss power model based on activities. **(10 Marks)**

4 a. Compare power estimation techniques based on simulation and probability theory. Draw the flow diagram of power estimation. **(10 Marks)**

b. Given $y = x_1x_2 + x_1x_3$ where x_i, i = 1, 2, 3 are mutually independent. If $z = x_1\overline{x_2} + y$, then determine P(z) and P(y). **(06 Marks)**

c. Determine signal probability of f = ab + c using BDD. **(04 Marks)**

5 a. Demonstrate power saving at logic level with suitable examples through gate reorganization. signal getting and logic encoding techniques. **(12 Marks)**

b. Describe precomputation logic optimization with an example. **(08 Marks)**

6 a. Describe two different schemes of clock tree driving in the context of VLSI design with the help of figure. **(10 Marks)**

b. Define zero skew and tolerable skew. Explain the concept of tolerable skew in a typical synchronous system with a pipelined / parallel architecture. Identify two cases of clock skew resulting into proper tolerable skew. **(10 Marks)**

7 a. Explain power analysis and estimation technique at algorithm level. **(10 Marks)**

b. How do you optimize power consumption for design case like FIR filter? **(10 Marks)**

8 Write technical notes on the following:
a. Monte Carlo simulation.
b. Power estimation using entropy.
c. Sizing an inverter chain.
d. Low power digital cell library. **(20 Marks)**

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